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Simulation and Analysis of Multistage Grid Connected Inverter Topology for Solar PV Based System

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Abstract
In this paper multistage grid connected inverter for solar PV based system and the types of multilevel inverter are discussed. The conventional line commutated inverters have square shaped waveform of line current which generates high harmonics and also produces excessive heat which causes damage to the winding of transformer. Alternatively, multilevel inverter reduces harmonics and gives output current waveform which is almost sinusoidal in nature. Basically, multilevel converter technology is based on the synthesis of the ac voltage from several different voltage levels on the dc side. i.e. by increasing of DC voltages, the levels of the output increases, which produce a staircase wave which approaches the sinusoidal wave with lower harmonic distortion. In the present work, a multilevel line commutated inverter topology has been proposed and analysed which improves the wave shape and hence reduces the total harmonic distortion (THD) of the line current in a grid connected line commutated inverter. Moreover, the performance of the proposed topology is far better than the conventional line-commutated inverter. The simulation is carried out in MATLAB/SIMULINK environment.
Keywords: Multilevel inverter, total harmonic distortion, grid connected inverter

I. INTRODUCTION

Growing scarcity and rising prices of fossil fuel may lead to economic instability in the future. These problems can be solved by the use of renewable energy resources. Most of the countries recognized the new energy policy to encourage the investment in photovoltaic energy system which is one of the biggest renewable resources in the world. Now days, solar energy is widely used for power generation. Because it has lot of advantages, i.e. Energy independence, Environmentally friendly, Required "Fuel" is already distribute freely everywhere, It needs minimum maintenance, Maximum reliability, and these systems are easily expanded [1]. The reducing cost of solar module and developments in power electronic devices makes solar power easily useful for power generation in bulk amount [2] but solar module gives the square wave shaped current wave. A single stage converter has 48% THD for perfect square wave of current [3]. In the present work, three level line-commutated inverter circuits have been developed and implemented with improved THD. It does away with the disadvantages associated with a conventional square wave inverter.

II. MULTILEVEL INVERTER

For providing electricity to grid, the supply should have low amount of harmonics. But the solar PV based system is having output of square wave shape. And as we know pure square wave contains 48% THD. So to reduce this amount, multilevel inverter is used. Multilevel inverter gives stepped wave output which is nearly sinusoidal in nature. So, multilevel inverter is used as grid connected inverter for solar PV based system.

A. Diode-Clamped Multilevel Inverter

The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter [4]. A three-phase six-level diode-clamped inverter is shown in Figure 1. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is V_{dc}, and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes. Table 1 lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage V_0 as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair require that the other complementary switch be turned off. The complementary switch pairs for phase leg a are (S_{a1}, $S_{a'1}$), (S_{a2}, $S_{a'2}$), (S_{a3}, $S_{a'3}$), (S_{a4}, $S_{a'4}$), and (S_{a5}, $S_{a'5}$). Table 1 also shows that in a diode-clamped inverter, the switches that are on for a particular phase leg is always adjacent and in series. For a six-level inverter, a set of five switches is on at any given time.

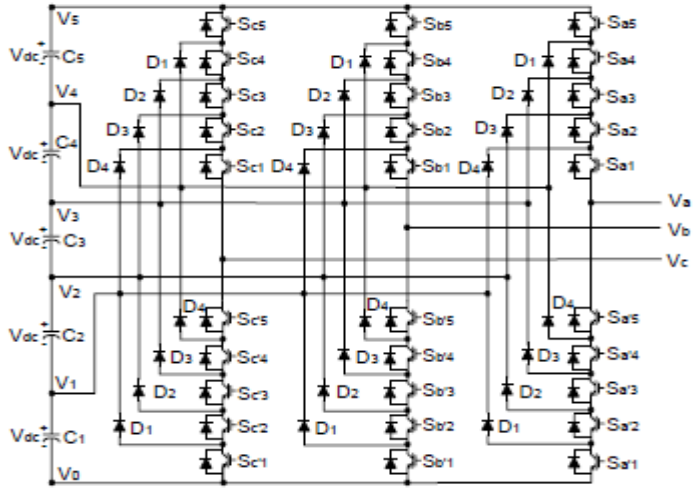

Fig. 1. Three-phase six-level diode-clamped inverter

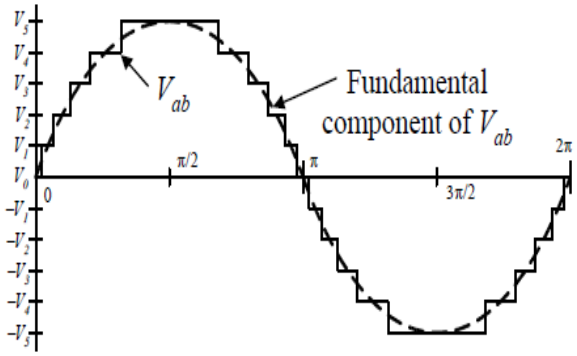

Fig. 2. Line voltage waveform

Table 1. Diode clamped six level inverter voltage level and corresponding switch state

Voltage V_{a0}	Switch State									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
V_5 = 5Vdc	1	1	1	1	1	0	0	0	0	0
V_4 = 4Vdc	0	1	1	1	1	1	0	0	0	0
V_3 = 3Vdc	0	0	1	1	1	1	1	0	0	0
V_2 = 2Vdc	0	0	0	1	1	1	1	1	0	0
V_1 = Vdc	0	0	0	0	1	1	1	1	1	0
V_0 = 0	0	0	0	0	0	1	1	1	1	1

Figure 2 shows one of the three line-line voltage waveforms for a six-level inverter. The line voltage V_{ab} consists of a phase-leg a voltage and a phase-leg b voltage. The resulting line voltage is an 11-level staircase waveform. This means that an m-level diode-clamped inverter has an m-level output phase voltage and a (2m-1)-level output line voltage.

Advantages

- All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection or an adjustable speed drive.
- The capacitors can be pre-charged as a group.
- Efficiency is high for fundamental frequency switching.

Disadvantages

- Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.
- The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels.

B. Flying Capacitor Multilevel Inverter

Meynard and Foch introduced a flying-capacitor-based inverter in 1992 [5]. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The circuit topology of the flying capacitor multilevel inverter is shown in Figure 3. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform.

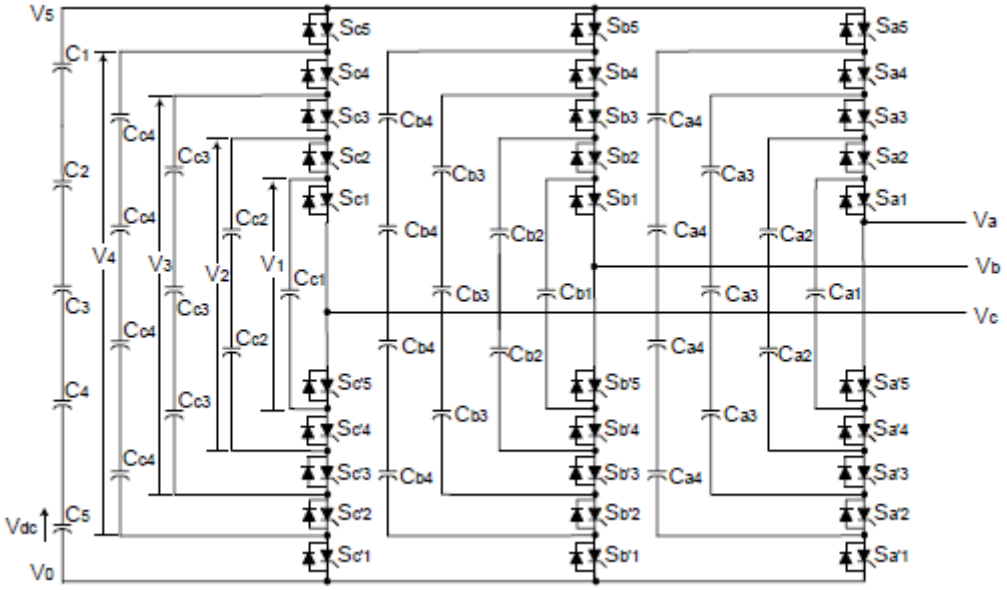

Fig. 3. Three-phase six-level structure of a flying capacitor inverter

One advantage of the flying-capacitor-based inverter is that it has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage. Table 2 shows a list of all the combinations of phase voltage levels that are possible for the six-level circuit shown in Figure 3. Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are on (conducting) be in a consecutive series. Moreover, the flying-capacitor inverter has phase redundancies, whereas the diode-clamped inverter has only line-line redundancies [6, 7, 8]. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels.

In addition to the (m-1) dc link capacitors, the m-level flying-capacitor multilevel inverter will require (m-1)×(m-2)/2 auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches. One application proposed in the literature for the multilevel flying capacitor is static var generation [6, 7]. The main advantages and disadvantages of multilevel flying capacitor converters are as follows [6, 7].

Table 2. Flying-capacitor six-level inverter redundant voltage levels and corresponding switch states

Voltage V_{a0}	Switch State									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_{a0} = 5V_{dc}$ (no redundancies)										
$5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$V_{a0} = 4V_{dc}$ (4 redundancies)										
$5V_{dc} - V_{dc}$	1	1	1	1	0	0	0	0	0	1
$4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc}$	1	0	1	1	1	0	1	0	0	0
$5V_{dc} - 3V_{dc} + 2V_{dc}$	1	1	0	1	1	0	0	1	0	0
$5V_{dc} - 2V_{dc} + V_{dc}$	1	1	1	0	1	0	0	0	1	0
$V_{a0} = 3V_{dc}$ (5 redundancies)										
$5V_{dc} - 2V_{dc}$	1	1	1	0	0	0	0	0	1	1
$4V_{dc} - V_{dc}$	0	1	1	1	0	1	0	0	0	1
$3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc} - V_{dc}$	1	0	1	1	0	0	1	0	0	1
$5V_{dc} - 3V_{dc} + V_{dc}$	1	1	0	0	1	0	0	1	1	0

$4V_{dc} - 2V_{dc} + V_{dc}$	0	1	1	0	1	1	0	0	1	0
$V_{a0} = 2V_{dc}$ (6 redundancies)										
$5V_{dc} - 3V_{dc}$	1	1	0	0	0	0	0	1	1	1
$5V_{dc} - 4V_{dc} + V_{dc}$	1	0	0	0	1	0	1	1	1	0
$4V_{dc} - 2V_{dc}$	0	1	1	0	0	1	0	0	1	1
$4V_{dc} - 3V_{dc} + V_{dc}$	0	1	0	0	1	1	0	1	1	0
$3V_{dc} - V_{dc}$	0	0	1	1	0	1	1	0	0	1
$3V_{dc} - 2V_{dc} + V_{dc}$	0	0	1	0	1	1	1	0	1	0
$2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$V_{a0} = V_{dc}$ (4 redundancies)										
$5V_{dc} - 4V_{dc}$	1	0	0	0	0	0	1	1	1	1
$4V_{dc} - 3V_{dc}$	0	1	0	0	0	1	0	1	1	1
$3V_{dc} - 2V_{dc}$	0	0	1	0	0	1	1	0	1	1
$2V_{dc} - V_{dc}$	0	0	0	1	0	1	1	1	0	1
V_{dc}	0	0	0	0	1	1	1	1	1	0
$V_{a0} = 0$ (no redundancies)										
0	0	0	0	0	0	1	1	1	1	1

Advantages

- Phase redundancies are available for balancing the voltage levels of the capacitors.
- Real and reactive power flow can be controlled.
- The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

Disadvantages

- Control is complicated to track the voltage levels for all of the capacitors. Also, pre charging all of the capacitors to the same voltage level and start-up are complex.
- Switching utilization and efficiency are poor for real power transmission.
- The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also more difficult in inverters with a high number of levels.

III. PROPOSED SCHEME

A multilevel converter circuit with RLE load works in two modes of operation i.e. rectification mode and inverter mode. It works in inversion mode when the switching angle of each of the converter is greater than 90°. Here, a new multilevel circuit topology has been developed as shown in Figure 4. The dc load side has been isolated from the grid via multi winding transformer.

The circuit has been analysed and implemented for three level of line current and can be extended to higher levels for better performance. But the increase of level adds to the cost of converter and more number of secondary windings. So, a suitable compromise has to be made between the THD of the line current and cost of additional hardware. When the circuit works in inverter mode, the dc source transfers power to the main (ac source). The major advantage of the proposed configuration is that in continuous current mode of operation, the waveform resembles a stepped sinusoidal wave and with suitable se- lection of switching angles the harmonic contents can be reduced drastically.

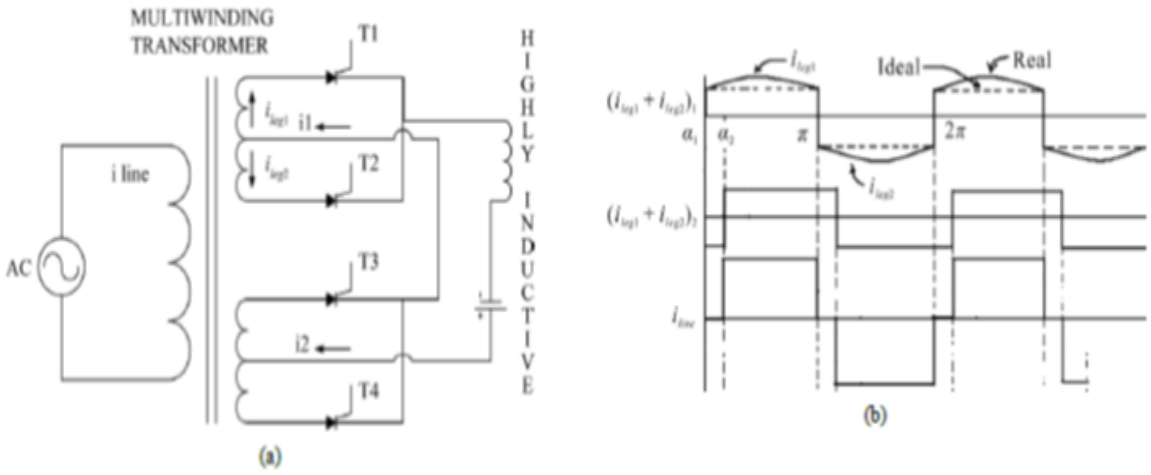

Fig. 4. Proposed multilevel converter circuit topology and its waveform (a) Circuit (b) load current of each converter and input line current

IV. CONTROL STRATEGY

In general, the load current can be either continuous or discontinuous. In the case of continuous current operation the current of both thyristors overlaps. It depends on dc source voltage, phase angle of load or inductor (φ) and the switching angle.

Three level control strategy: For three level line current, a set of secondary winding with centre tap arrangement is required. Each pair of thyristor in a centre tap secondary is fired at a switching delay of 180˚. The upper leg thyristor is fired at angle greater than 90˚ for inversion operation. Simultaneously lower leg thyristor is fired at a delay of 180˚ with respect to the upper leg thyristor.

The expression of the converter current is obtained by solving the equation

$$L\frac{di}{dt} + iR = V_m \cos\omega t + E \qquad (1)$$

For $\omega t = \theta$ and $m = \left(\frac{E}{V_{leg1}}\right)$, it gives i_{leg1} for conduction through T_1 in positive half cycle in upper leg of converter.

$$i_{leg1} = \cos(\theta-\varphi) + \frac{m}{\cos(\varphi)} * \left(1 - e^{\frac{1(\theta-\varphi)}{\tan(\varphi)}}\right) - \cos(\theta-\varphi) * e^{\frac{1(\theta-\varphi)}{\tan(\varphi)}} \qquad (2)$$

For conduction through T_2 in negative half cycle, the expression of lower leg converter current is given by

$$i_{leg2} = -\cos(\theta-\varphi-\pi) - \frac{m}{\cos(\varphi)} * \left(1 - e^{\frac{1(\theta-\varphi-\pi)}{\tan(\varphi)}}\right) + \cos(\theta-\alpha) * e^{\frac{-1(\theta-\alpha-\pi)}{\tan(\varphi)}} \qquad (3)$$

Each converter contributes to the line current and the net line current, i_{line}, is equal to the sum of all $(i_{leg1} + i_{leg2})_n$. n = 1, 2.

V. SIMULATION RESULTS

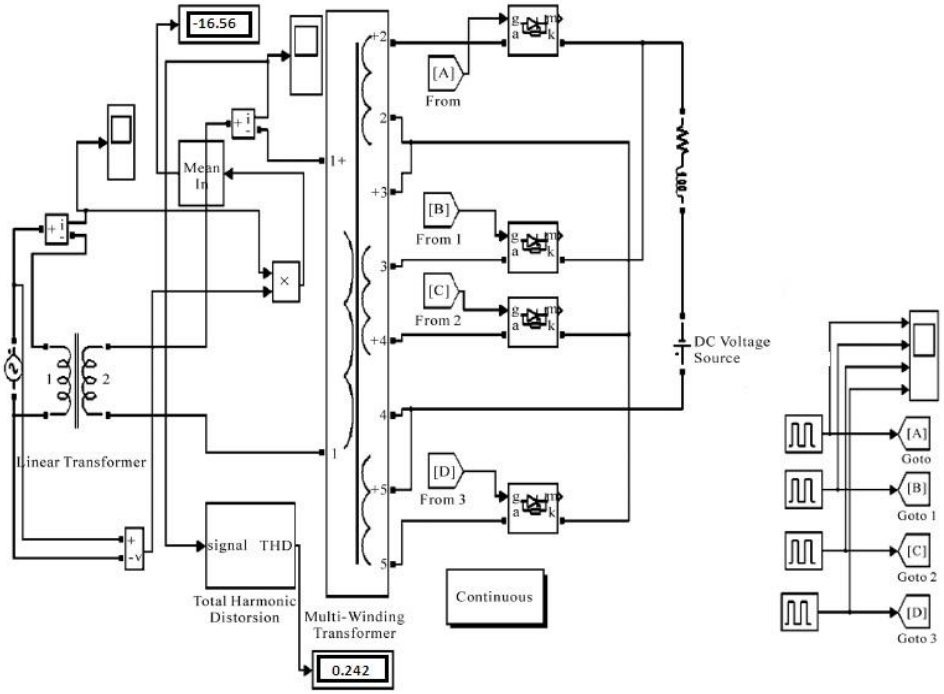

Fig. 5. SIMULINK model of the three step line commutated inverter

VI. CONCLUSION

Multilevel inverter for three levels is successfully implemented. We found that, by increasing level of inverter, THD of the line current of the grid-tie multilevel inverter has been reduced to 32.84% (instead of 48% for conventional line commutated inverter). If proper filter circuit is used, THD can be reduced further. With reduced THD, multilevel inverter can be a better substitution for square wave inverter in various solar PV based system.

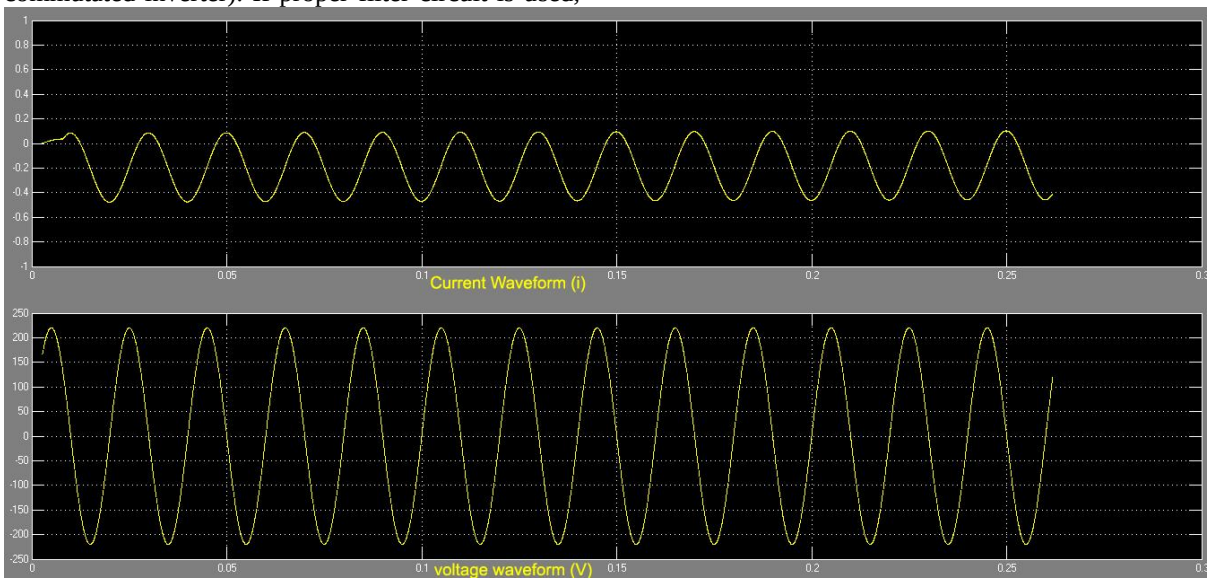

Fig. 6. Line current and Voltage.

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